AMENDMENTS TO THE CLAIMS

1. (currently amended): An optoelectronic sensor comprising:

at least one photodiode having a photodiode capacitance; ~~(1) which can be connected to a first potential ($V_{reset,}$ V_{reset1}) via~~

a first transistor ~~(T1)~~ or a first diode ~~(D1)~~ connected between said photodiode and a first potential, said first transistor having a channel and a gate connected to a first gate voltage; ~~,~~

a readout amplifier having an input and an output;

a storage means connected to the input of said readout amplifier to allow temporary storage of a signal value at the input of the readout amplifier during a holding time and until a readout time;

~~characterized in that~~

a second transistor connected between said photodiode and the input of said readout amplifier in order to provide a large dynamic range, said second transistor having a gate connected to a second gate voltage; ~~,~~ and~~the photodiode (1) can furthermore be connected to the input of a readout amplifier (T3) via a second transistor (T2),~~

a third transistor ~~(T5) via which~~ connected between the input of the readout amplifier ~~(T3) can be connected to~~and a second potential ~~($V_{reset,}$ V_{reset2}) furthermore being arranged between the second transistor (T2) and the input of the readout amplifier (T3), and~~

~~in that there are means (C2) which allow temporary storage of the integrated signal value until the readout time~~

the optoelectronic sensor being operable to change said signal value at the input at the readout amplifier due to light impinging on said photodiode during an integration time, the integration time having at least a first and a last phase,

wherein said second gate voltage is controllable so that a current generated by the photodiode discharges only said storage means in the first phase of the integration time, and

wherein the first gate voltage if there is a first transistor, or the first potential if there is a first diode, is controllable so that some or all of the current generated by the photodiode is compensated for by the channel of the first transistor or by the first diode, respectively, in the last phase of the integration time.

2. (currently amended): The optoelectronic sensor as claimed in claim 1, ~~characterized in that~~ wherein there is a first transistor ~~(T1)~~, and ~~in that~~ wherein the first and second potentials ~~(V_{reset})~~ are at an essentially identical voltage level.

3. (currently amended): The optoelectronic sensor as claimed in claim 1, ~~characterized in that~~ wherein said storage means comprise a ~~an additional~~ conversion node ~~capacitor~~ capacitance connected ~~(C2) to ground potential (2) is arranged~~ between ~~the second transistor (T2) and~~ the input of the readout amplifier ~~(T3)~~ and a ground potential.

4. (currently amended): The optoelectronic sensor as claimed in claim 1, ~~characterized in that~~ further comprising a row selection transistor and a column bus, the output of the readout amplifier ~~(T3) is~~ being connected to ~~a~~ the column bus via ~~a~~ the row selection transistor ~~(T4)~~.

5. (currently amended): The optoelectronic sensor as claimed in claim 1, ~~characterized in that~~ wherein at least one~~, and preferably all~~ of the transistors ~~(T1, T2, T3, T4, T5) used are designed as~~ is a MOS ~~transistors~~ transistor.

6. (cancelled).

7. (currently amended): The optoelectronic sensor as claimed in claim ~~6~~1, ~~characterized in that in the case of a~~ wherein there is a first transistor, wherein ~~(T1)~~ the first gate voltage ~~of the first transistor (T1)~~ is lower than the second gate voltage, ~~of the second transistor (T2)~~ and ~~in that~~ wherein the first gate voltage ~~of the first transistor (T1)~~ is higher than ~~the~~ a saturation signal of the readout ~~buffer~~ amplifier at least by a threshold voltage~~, or respectively in that in the case of a first diode (D1) the diode anode voltage of the first diode (D1) is adjusted by the first potential (V_{reset1}) so that this anode voltage minus the diode threshold voltage ($V_{reset1} - V_{onDiode}$) is lower than the gate voltage minus the threshold voltage of the second transistor (T2) and in that the diode anode voltage (V_{reset1}) of the first diode (D1) is higher than the saturation signal of the readout buffer at least by a diode threshold voltage ($V_{onDiode}$)~~.

8. (currently amended): The optoelectronic sensor as claimed in claim ~~6~~1, ~~characterized in that the~~ wherein said first and second transistor each have a threshold voltage, said threshold voltage having a tolerance, wherein said first and second gate voltage have a tolerance, and wherein said first and second gate voltage are selected such that there is a difference between the ~~two~~ first and second gate voltages, said difference being ~~is~~ greater than the tolerances of the threshold voltages plus the tolerances of the first and second gate voltages ~~values, this difference particularly preferably being selected to be > 100 mV~~.

9. (currently amended): The optoelectronic sensor as claimed in claim 1, ~~characterized in that~~ wherein the first and second gate voltages of the first transistor ~~(T1)~~ and of the second transistor ~~(T2) can be varied~~ are variable during the integration time.

10. (currently amended): A method for operating an optoelectronic sensor, said sensor comprising:

at least one photodiode having a photodiode capacitance;

a first transistor or a first diode connected between said photodiode and a first potential, said first transistor having a channel and a gate connected to a first gate voltage;

a readout amplifier having an input and an output;

a conversion node capacitance connected to the input of said readout amplifier to allow temporary storage of a signal value at the input of the readout amplifier during a holding time;

a second transistor connected between said photodiode and the input of said readout amplifier, said second transistor having a gate connected to a second gate voltage; and

a third transistor connected between the input of the readout amplifier and a second potential,

~~as claimed in claim 1, characterized in that~~ the method comprising controlling the first gate voltage ~~of the~~ if there is a first transistor ~~(T1),~~ or ~~respectively~~ the first potential ~~(V_{reset1})~~ ~~in the case of a~~ if there is a first diode ~~(D1),~~ and controlling the second gate voltage of the second transistor, during an integration time, the integration time preceding the holding time and having a first, a second and a third phase, ~~(T2), is respectively adjusted or controlled~~ so that charge

carriers accumulated by the photodiode ~~(1)~~ discharge only ~~a~~ said conversion node ~~capacitor~~ capacitance ~~(C2)~~ in ~~a~~ the first phase of the integration time, ~~in~~ that charge carriers accumulated by the photodiode ~~(1)~~ discharge both ~~a~~ the photodiode ~~capacitor~~ capacitance ~~(C1)~~ and said conversion node ~~capacitor~~ capacitance ~~(C2)~~ in ~~a~~ the second phase of the integration time, the second phase beginning after an equal potential has been reached at the output of the photodiode ~~(1)~~ and at the input of the readout amplifier ~~(T3)~~, and ~~in~~ that after the output of the photodiode ~~(1)~~ has fallen below the threshold value of the first transistor ~~(T1)~~ or ~~respectively~~ the diode threshold value of the first diode ~~(D1)~~, charge carriers accumulated by the photodiode ~~(1)~~ are at least partially made available via the first transistor ~~(T1)~~ or ~~respectively~~ via the first diode ~~(D1)~~ in ~~a~~ the third phase of the integration time ~~,~~

~~and in that said second transistor (T2) is opened after the integration time has elapsed so that the signal is held at the conversion capacitor (C2) until the readout time and in that the first transistor (T1) or respectively the first diode (D1) is adjusted during this holding time so that the photodiode capacitor (C1) is not fully discharged~~.

11. (currently amended): The method as claimed in claim 10, ~~characterized in that~~ wherein the gate voltage of the second transistor ~~(T2)~~ is adjusted during ~~the~~ a reset ~~phase~~ time and during the integration ~~phase~~ time so that the second gate voltage minus ~~the~~ a threshold voltage of the second transistor is lower than ~~the~~ a reset voltage which is set at the input of the readout amplifier ~~(T3)~~, and ~~in that~~ wherein the second gate voltage is higher than ~~the~~ a saturation voltage of the readout buffer at least by a threshold voltage.

12. (currently amended): The method as claimed in claim 10, ~~characterized in that~~ wherein the second gate voltage ~~of the second transistor (T2)~~ is varied during the integration ~~phase~~ time, although it always remains greater than the first gate voltage ~~of the first transistor (T1), and in that the gate voltage of the first transistor (T1) is preferably reduced successively during the integration phase~~.

13. (currently amended): The method as claimed in claim 10, ~~characterized in that~~ wherein the first gate voltage ~~of the first transistor (T1)~~ is kept constant or successively reduced during the integration time.

14. (currently amended): The method as claimed in claim 10, ~~characterized in that~~ wherein the second gate voltage ~~of the second transistor (T2)~~ is switched at least once so that it is equal to ~~the~~ a bulk potential of ~~this~~ the second transistor ~~(T2)~~ and is switched back again to its original value.

15. (previously presented): A one- or two-dimensional array of optoelectronic sensors as claimed in claim 1.

16. (previously presented): A method according to claim 10 for operating an array as claimed in claim 15.

17. (new): The optoelectronic sensor as claimed in claim 1, wherein the integration time has a second phase between the first phase and the last phase, the second phase beginning after an equal potential has been reached at the output of the photodiode and at the input of the readout amplifier, and wherein the optoelectronic sensor is operable in said second phase of the integration time so that charge carriers accumulated by the photodiode discharge both the photodiode capacitance and said conversion node capacitance until the output of the photodiode has fallen below the threshold value of the first transistor or the diode threshold value of the first diode.

18. (new): The optoelectronic sensor as claimed in claim 1, wherein said second transistor is operable to be opened at the end of the integration time so that a signal is held in the storage means during a holding time and until a readout time, wherein the first transistor or the first diode is operable to be adjusted during this holding time so that the photodiode capacitance is not fully discharged.

19. (new): The optoelectronic sensor as claimed in claim 1, wherein the first diode is present, wherein said first diode has a diode threshold voltage and a diode anode voltage, the diode anode voltage being adjustable by the first potential in a manner that the anode voltage minus the diode threshold voltage is lower than the second gate voltage minus a threshold voltage of the second transistor, and wherein the diode anode voltage is higher than a saturation signal of the readout amplifier at least by the diode threshold voltage.

20. (new): The method of claim 10, further comprising opening said second transistor after the integration time has elapsed so that the signal is held at the conversion node capacitance during the holding time and until a readout time, wherein the first transistor or the first diode is adjusted during this holding time so that the photodiode capacitance is not fully discharged.